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# Self-controlled fabrication of single-crystalline silicon nanobeams using conventional micromachining

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## Abstract

This paper reports on a low-cost top-down approach to the nano-precision fabrication of nanobeams on single-crystalline silicon using only conventional micromachining technology. The fabrication technique takes advantage of the crystalline structure of silicon for controllable feature size reduction of nanobeams with atomically smooth surfaces and sharp edges. Applying a deliberate rotational misalignment in a 2  $\mu\text{m}$  resolution standard lithography process, followed by anisotropic wet etching of the silicon, nanobeams with well uniform widths as small as  $\sim 85$  nm are fabricated on thin SOI substrates. As a proof of concept for the incorporation of such nanobeams within electromechanical structures, we successfully demonstrate thermally actuated resonators that show very high frequencies (close to 50 MHz).

Keywords: top-down batch fabrication, single-crystalline structure, silicon nanobeam, standard lithography, thermal-piezoresistive electromechanical resonator

(Some figures may appear in colour only in the online journal)

## 1. Introduction

A great deal of attention has been paid to silicon nanowalls/nanowires in nanoelectronics [1–3], nanophotonics [4–6], biochemistry [7–9] and nano-electromechanical devices [10–12] within the past few decades. When silicon nanowires shrink, their electrical and optical properties deviate considerably from those of bulk Si, in particular, at diameters close to the wavelength of the electron wave function where the quantum confinement effects begin to dominate [13–16]. Huge scattering and absorption efficiencies, low leakage current, good control over short-channel effects and giant piezoresistive coefficients are among the distinctive properties of Si nanowires observed at minuscule scales; due to larger ionization energy; this has helped to usher in a new era in the development of ultimate electronic and optoelectronic devices and sensors. A recent study conducted on thermal-piezoresistive MEMS resonators also revealed that embedded with

scaled-down actuator beams (practically nanowires), ultra high frequencies in the GHz range and low power consumptions in the sub-milliwatt range is realizable for thermally actuated devices [17].

Nonetheless, despite numerous efforts devoted to developing different top-down and bottom-up techniques, difficulties still remain regarding the controlled batch fabrication of well-defined nano-structures. Over the past decade, substantial progress in the fabrication of silicon nanowires using bottom-up processes has been made [18–20]. However, such approaches do not allow for control over the number and position of grown nanowires, and the complicated assembly procedures are required after fabrication. Integration of individual nanowires into the macroscopic world, reproducibility and uniformity of growth are among the other challenges associated with such techniques. In effect, bottom-up nanowires are conventionally grown as entangled meshes and, as a result, lack the predetermined ordering that is essential to integrate individual nanowires into electromechanical devices. Despite recent advances in extracting nanowires from such entangled meshes and aligning them on

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substrates, such techniques are still not suitable for the mass production of nanowires that is required in many applications [20].

On the other hand, top-down fabrication approaches [20–25], among which E-beam lithography (EBL) is the most commonly used, involve producing high resolution masks on thinned-down silicon substrates and then etching away the unwanted parts in order to create desired nanoscale features. Despite allowing for control over the number and position of the features, it is a time-consuming serial route which is not suitable for high-volume manufacturing. Other commonly encountered challenges associated with standard EBL processes include surface charging of insulating substrates throughout the electron-substrate interactions and undesirable size variations due to imperfect subsequent deep reactive ion etching (DRIE) processes.

In parallel with the continuing effort to overcome challenges associated with EBL technology, a number of low-cost techniques for the fabrication of nanowires/nanowalls that utilize standard lithography have already been reported. In the simplest approach, a number of consecutive thermal oxidation and oxide removal steps can be performed on microscale structures to thin down the structural components that lead to nanoscale features [26]. This technique, however, results in severely rounded and unpredictable features, deteriorating device performance and uniformity in a batch. In order to reduce the effect of round corners/rough edges and non-uniformities in a more effective way, the width of the initially patterned photoresist was first reduced by feeding a mixture of  $\text{He/O}_2 + \text{N}_2$  in a plasma etch step. After forming the SiNWs, a thermal oxidation step was also performed to further shrink down the dimensions of the SiNWs [12]. In another approach [27], which took advantage of the silicon crystalline structure, a two-mask microfabrication process was used on (100) SOI wafers to fabricate sub-30 nm-wide Si-NWs. In this technique, two lithography and anisotropic wet etch steps were used to form Si-NWs with isosceles triangular cross sections. Although an interesting and powerful technique, misalignment between the two lithography steps introduced challenges regarding the incorporation of such nanowires into more sophisticated structures. More recently, a single-step standard lithography, followed by deep silicon etch and anisotropic wet etch processes, was employed, which formed inverted triangle-shaped Si wires [28]. To reduce the dimensions of the Si wires down to sub-100 nm, however, traditional thermal oxidation, followed by an oxide removal step, was performed. A similar technique [29] was also used on (111) silicon substrates, which led to inclined silicon nanowalls that were as narrow as 350 nm. Still, to further scale down the features, a thermal oxidation approach was used; this approach demonstrated nanowires with lateral dimensions as small as 60 nm.

Herein, a simple, versatile and highly controlled nanoprecision batch nanobeam/nanowire fabrication scheme that is capable of integration within macro, micro and nanoscale electromechanical systems, as well as interconnects, is introduced. The presented technique only works based on a deliberate rotational misalignment, which is introduced

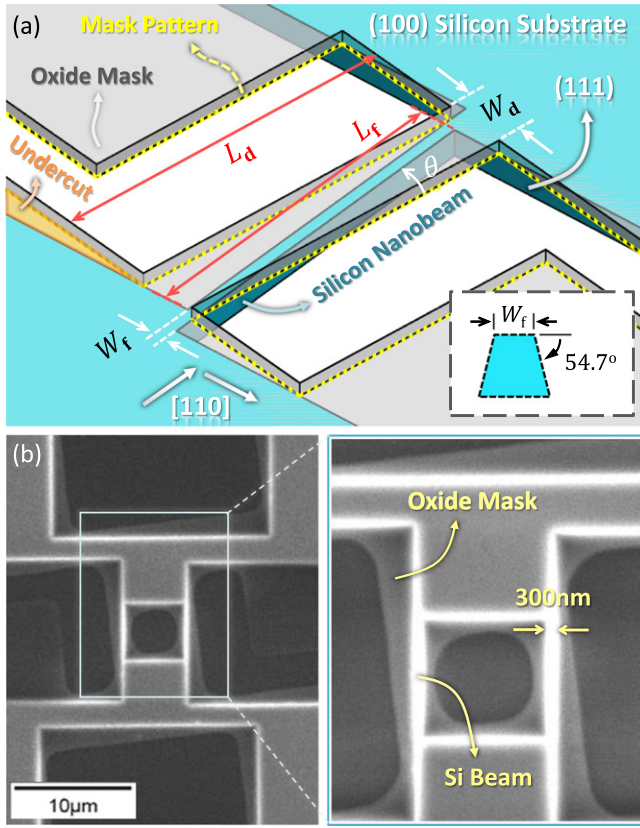
between the photo-lithography patterns and the crystal orientation of the silicon substrates. Using this approach, nanobeams, working as thermal actuator/piezoresistive sensors, are demonstrated within thermally actuated resonant structures.

## 2. Methods

Since its beginning in the early 1950's, anisotropic wet chemical etching of silicon has been extensively used and has now become a standard technology in semiconductor industry. More importantly, different wet etch rates in different crystallographic directions of silicon has been continuously exploited in order to devise novel fabrication technologies [30–32]. Due to different numbers of dangling bonds per unit cell within different directions in mono-crystalline Si, the etch rate of the (111) planes is considerably slower than that of the (110) planes [33]; thereby, (111) planes can act as strong etch-stops when it comes to wet-etching processes. Taking advantage of the same principle, a single-mask photo-lithography step is utilized here to turn the microscale patterns into nano-sized features on the crystalline silicon-on-insulator substrates (SOI). After introducing an intentional rotational misalignment  $\theta$  between the micro-precision patterns and the (110) planes on the (100) substrate, the alkaline solution begins to undercut the hardmask, while the very first (111) planes that are fully covered by the hardmask act as etch stops throughout the wet chemical etch process (see figure 1(a)). Allowing for an appropriate etch time, the resulting undercut can lead to much smaller feature sizes on the ultimate silicon structure (figure 1(b)). The etching ratio of  $>600$  to 1 in the  $\langle 110 \rangle$  to  $\langle 111 \rangle$  [33] provides a high degree of controllability over the ultimate feature sizes that are obtained after an appropriately timed wet etch process.

The key advantage of such an undercut over undercuts caused by isotropic etch processes is its self-control and relative independence from the etch rate and the timing of the process [34]. Utilizing the same photomask, such a technique can also provide flexibility over the ultimate feature sizes by merely changing the initially introduced misalignment angle. Furthermore, the rounded corners and the rough edges in the photolithographically defined hardmask turn into sharp corners and smooth edges within the resulting wet-etched silicon structure (see figure 1(b)). For the sake of comparison, the outcome of the presented approach is illustrated in figure 2(a), along with a similar nanobeam-based structure obtained through DRIE, followed by successive thermal oxidation and oxide removal steps (figure 2(b)). The harshly rounded and unpredictable features on the structure in figure 2(b) clearly show the advantage of the presented wet-etch/feature-reduction technique, which results in atomically precise and extremely smooth surfaces (figure 2(a)).

As described earlier, the dimensions of the ultimate structure are controlled by the angle introduced between the original pattern and the appropriate crystallographic direction (110 in the case of 100 Si substrates) and the size of the microscale defined patterns. The final dimensions of the



**Figure 1.** (a) 3D Schematic view of the self-controlled approach for the fabrication of a nanoscale Si beam using standard photolithography; this approach introduces a rotational misalignment angle between the microscale patterns and the crystallographic direction of the Si substrate. The inset shows the cross-sectional view of the Si nanobeam. (b) Top SEM view of a wet chemical etched Si structure, along with its angled microscale hardmask, which clearly indicates the size scale-down, as well as the edge sharpening within the Si structure.

narrow silicon beam in figure 1(a) can be determined using the following equations:

$$L_f = L_d \cos \theta - W_d \sin \theta \quad (1)$$

$$W_f = W_d \cos \theta - L_d \sin \theta \quad (2)$$

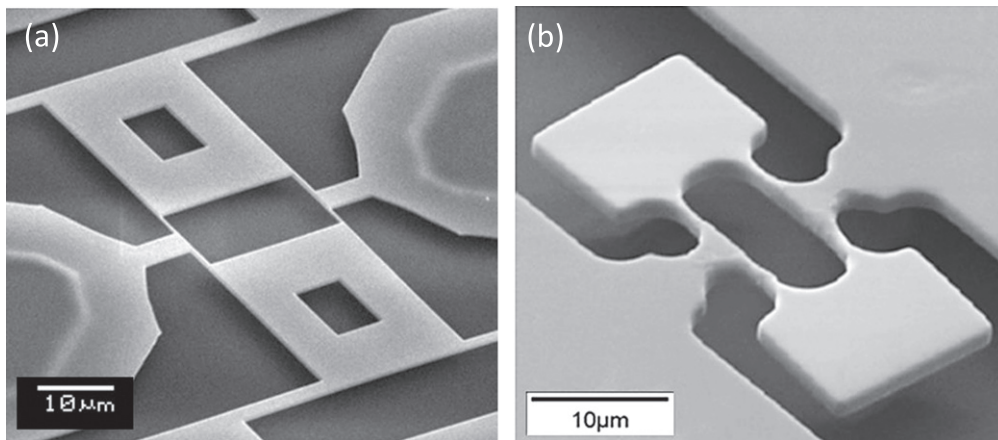
where  $L_d$  and  $W_d$  are the initially defined dimensions on the hardmask,  $L_f$  and  $W_f$  are the dimensions of the resulting Si beam and  $\theta$  is the intentionally induced misalignment angle (denoted in figure 1(a)). The sensitivity of the ultimate feature size to the misalignment angle is:

$$\frac{\partial W_f}{\partial \theta} = -L_d \sin \theta - W_d \cos \theta \quad (3)$$

For example, in order to fabricate a nanowire with a width and a length of 50 nm and 2  $\mu\text{m}$ , respectively, using a 1  $\mu\text{m}$  photolithography resolution, the sensitivity of the ultimate width of the nanowire to the rotational misalignment would be 47 nm/degree. Therefore, to attain an accuracy of 2 nm, a precision of 0.04 degrees will be needed, which can be easily realized using regular mask alignment systems.

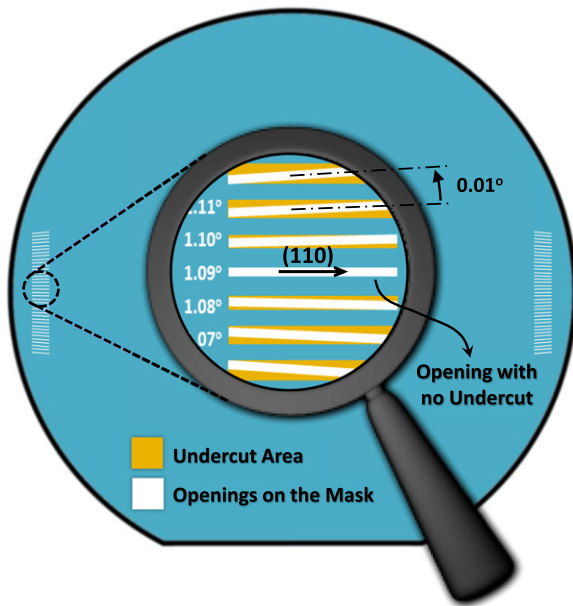
Prior to starting the fabrication process, it is necessary to accurately identify the (110) direction on the silicon substrate [35]. A silicon oxide layer was thermally grown and patterned with an array of long narrow openings (2  $\mu\text{m} \times 2000 \mu\text{m}$ ) that were rotated with a tiny angular increment of 0.01 degree with respect to each other (figure 3). After an appropriately time anisotropic wet etch of the silicon substrate in the KOH, all of the openings that had a misalignment with respect to the (110) plane were undercut, among which the one with the smallest amount of, or possibly no, undercut indicated the 110 direction with 0.01 degree precision. The appropriate misalignment angle for achieving the desired ultimate feature size can therefore be easily realized by selecting the proper alignment mark (opening with the appropriate misalignment angle) on the oxide hardmask.

The process continued with the previously grown silicon oxide layer on top of the (100) SOI wafers. A standard photolithography step with 2  $\mu\text{m}$  resolution was first performed with the desired misalignment angle (figure 4(a)). The silicon device layer was then etched in an alkaline solution (KOH here) for an appropriate period of time to form the ultimate features in a self-controlled fashion (figure 4(b)). After the oxide removal step in hydrofluoric acid (HF), the



**Figure 2.** (a) A nanobeam embedded electromechanical structure that was fabricated with very sharp edges and high-quality defined components using the presented technique. (b) A similar structure with nano-features that is defined with consecutive thermal oxide growth and HF removal steps and shows severely rough and unpredictable features.



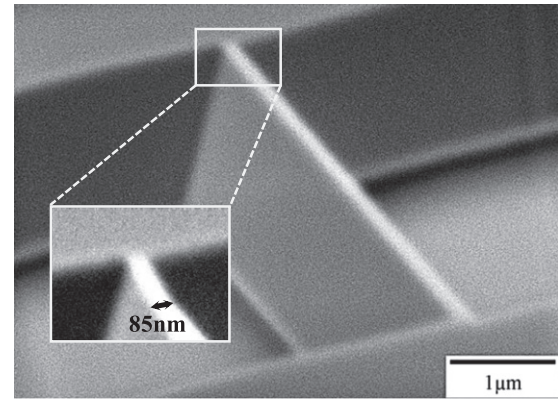


**Figure 3.** Schematic of the technique used to determine the (110) direction with 0.01 degree precision on the Si wafers. An array of long narrow openings ( $2\ \mu\text{m} \times 4000\ \mu\text{m}$ ) with an angular increment of 0.01 degree was patterned on a thermally grown oxide mask. After a suitably timed anisotropic wet etching of silicon in an alkaline solution (e.g., KOH), undercuts as big as at least 700 nm, easily visible using an optical microscope, were generated at two diagonal corners of each feature, except the one that was aligned to (110) direction degrees.

resulting structure had narrower components compared to the originally defined mask pattern (figure 4(c)).

### 3. Results and discussions

SOI substrates with thin device layers (500 nm– $2\ \mu\text{m}$ ) were used to fabricate thermally actuated resonant structures that were integrated with thermal actuator/piezoresistive sensor nanobeams. The SEM view of an 85 nm-wide nanobeam with a trapezoidal cross-section, which was fabricated on a  $2\ \mu\text{m}$ -

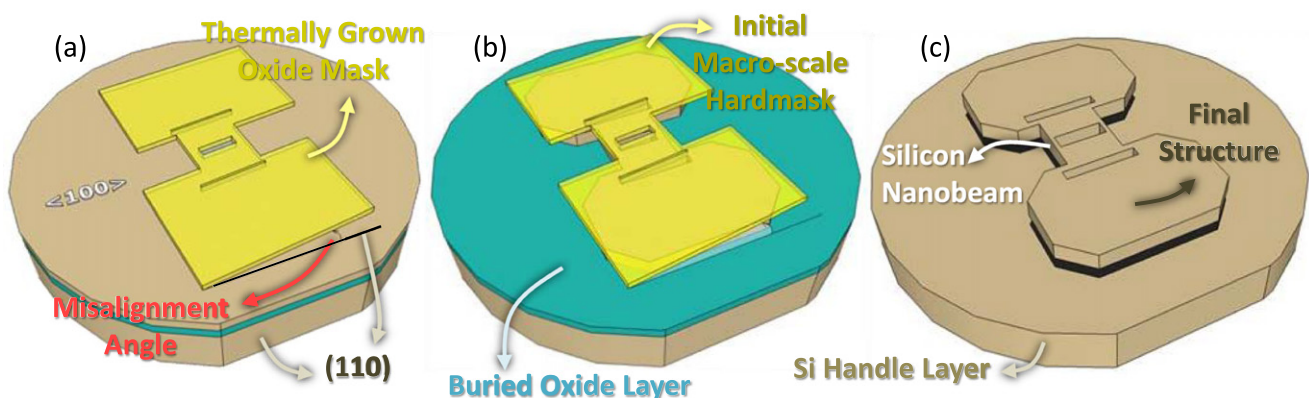


**Figure 5.** SEM view of a suspended silicon nanobeam with a width of ~85 nm that was fabricated on a  $2\ \mu\text{m}$ -thick device layer silicon substrate.

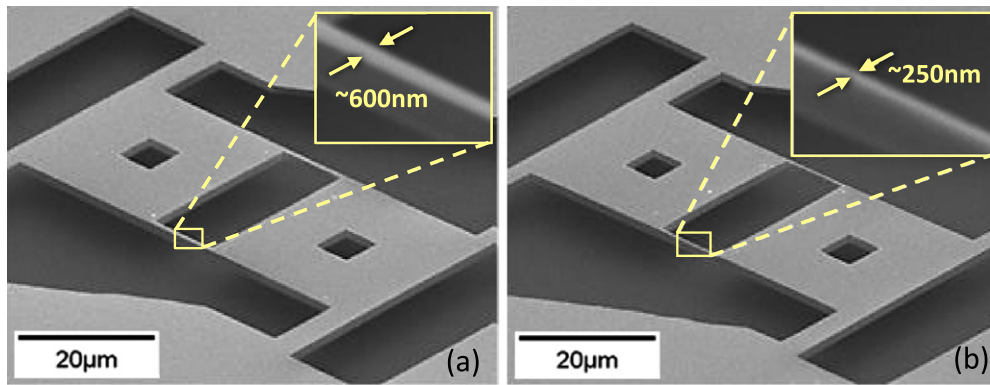
thick silicon substrate using the presented technique, is illustrated in figure 5.

As previously discussed, the dimensions in the ultimate structure can be determined by the misalignment angle that was introduced during the photolithography step. Generally speaking, a larger misalignment angle results in smaller final dimensions. Two similar electromechanical resonant structures that were patterned using the same lithography mask, but with different angles fabricated on a  $2\ \mu\text{m}$ -thick Si substrate, are shown in figure 6. The structure that was fabricated with a 1 degree smaller misalignment angle lead to ~600 nm-wide beams (figure 6(a)), while the same feature on the other structure clearly has a smaller width of ~250 nm (figure 6(b)). Narrower beams could have been fabricated if a slightly larger angle had been induced. Two other dual-plate thermally actuated resonant structures that have different numbers of actuator beams and feature sizes as small as 150 nm, fabricated on a 500 nm-thick Si substrate, are illustrated in figure 7.

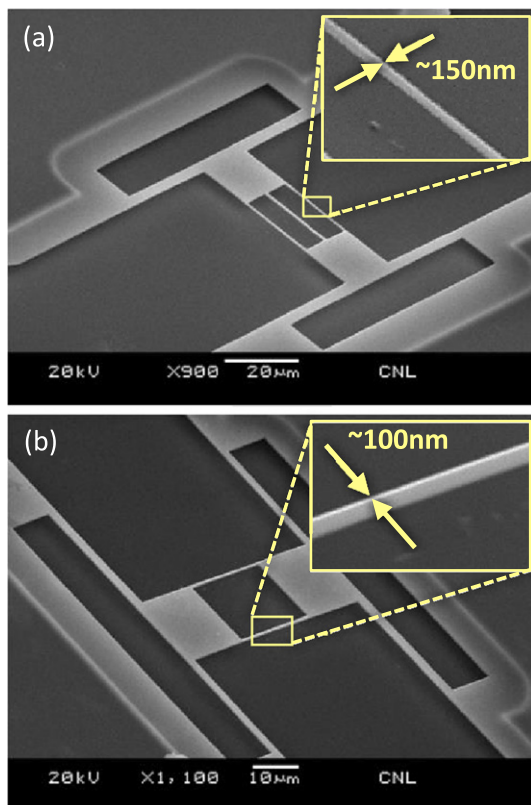
The fabricated thermally actuated resonant structures can be actuated simply by applying an ac voltage between the two support pads on their two sides [17]. The resulting current passes through the structure, thereby heating it up due to the resulting



**Figure 4.** Top-down microfabrication process flow for creating suspended silicon structures with nanoscale features on SOI substrates using a single mask photolithography process (skipping the crystallographic direction identification step). (a) Thermally grown and patterned oxide layer on a (100) silicon-on-insulator wafer using standard photolithography with the appropriate rotational misalignment. (b) An appropriately timed anisotropic wet etch of silicon in KOH. (c) Oxide removal and release of the structure in HF.



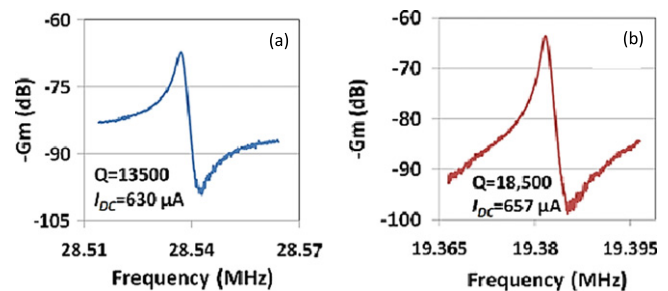
**Figure 6.** SEM views of two fabricated resonant structures with similar initial patterns but different induced angles that show much narrower actuator beams on the right side structure and are rotationally misaligned with a one degree greater difference during lithography.



**Figure 7.** Suspended resonant crystalline silicon structures fabricated on 500 nm-thick Si substrates using the described scale-down technique.

ohmic loss. The ohmic losses are maximized in the thinner parts, which are typically located on the narrow beams in the middle of the structure. The fluctuating power loss, as a result of the ac current, leads to a fluctuating temperature gradient and, therefore, leads to the periodic thermal expansion of the actuator beams. The alternating extensional force, resulting from the fluctuating temperature in the beams, can then actuate the resonator in its in-plane extensional resonance mode.

If the ohmic loss and, consequently, the resulting temperature fluctuations have the same frequency as the resonant frequency of the resonator, the mechanical vibration amplitude can be amplified by the mechanical quality factor  $Q$  of the

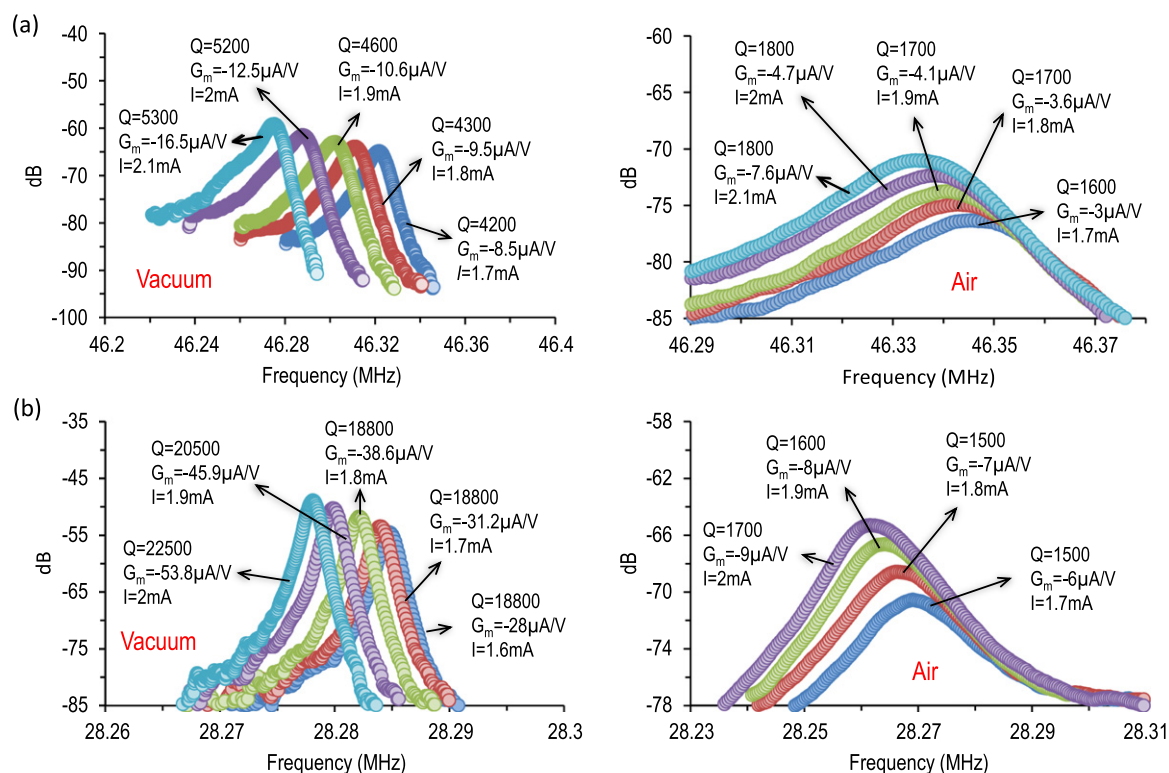


**Figure 8.** Measured frequency responses of (a) the 28.5 MHz resonator of figure 6(a). (b) The 19.4 MHz resonator of figure 6(b) both tested in vacuum.

resonator. The amplified alternating stress in the pillars leads to increased fluctuations in their electrical resistance (due to the piezoresistive effect). When biased with dc voltage, such resistance fluctuations modulate the current passing through the structure, resulting in an ac current component known as the motional current. The ratio of the motional current to the applied actuation voltage, called motional conductance, is one of the fundamental parameters for such devices.

Figure 8 compares the in-vacuum frequency responses of the two similar resonant structures in figure 6, which only differ in the width of the support beams. The vertical axis shows the absolute value of motional conductance in dB with reference to a  $1/50 \Omega$  conductance ( $20 \log(2 \times 50 \times g_m)$ ). As expected, with comparable bias currents, the resonance frequency of the resonator in figure 6(a) with wider beams is  $\sim 1.5 \times$  higher than that of the resonator in figure 6(b). This is due to the fact that the wider support and the actuator beams result in higher overall stiffness of the structure, and therefore results in higher resonance frequencies.

Figure 9 also shows different frequency responses for the resonators in figures 7(a) and (b) at different bias currents under vacuum and atmospheric pressure. The very thin actuator beams lead to clear resonance peaks with motional conductance of up to  $54 \mu\text{A V}^{-1}$  in vacuum and  $9 \mu\text{A V}^{-1}$  in air upon application of dc bias currents of only  $\sim 2 \text{ mA}$  and power consumption of  $\sim 9 \text{ mW}$ . As expected, upon increasing the dc bias current, the motional current level increases, while



**Figure 9.** Measured frequency responses under different bias currents for (a) the resonant structure in figures 7(a) and (b) the structure in figure 7(b). The graphs on the left show the results under a vacuum while the graphs on the right represent the results measured in air.

the resonator frequency decreases, due to the higher static temperature and the softening of the structural material.

#### 4. Conclusions

A nano-precision fabrication scheme for the high-volume manufacturing of silicon nanobeams, and possibly nanowires, using only standard micromachining techniques was introduced. This very low-cost and novel approach can be used for the highly controllable fabrication of nanoscale crystalline silicon electromechanical structures with atomically smooth interfaces. Sub-100 nm Si nanobeams on thin SOI substrates were successfully demonstrated using this approach. The fabricated nanobeams were operated as transducers in thermal-piezoresistive resonant structures, and their extremely high performance was demonstrated. The presented batch-fabrication technique could be applied to a variety of other systems, including nanoelectronic and optoelectronic devices. By employing thinner silicon substrates, nanowires can be practically fabricated using the same technique.

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