Deep submicron parallel scanning probe lithography using two-degree-of-freedom microelectromechanical systems actuators with integrated nanotips

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A new enabling technology for low-cost high throughput parallel scanning probe nanolithography is presented. Monolithic integration of microelectromechanical systems (MEMS) actuators with two-dimensional probe arrays as well as preliminary results in the simultaneous generation of multiple submicron patterns using such structures is reported. Two-degree-of-freedom electrothermal MEMS positioning structures integrated with nanoscale probe-tips are used to perform parallel scanning probe nanolithography circumventing the main deficiency of tip-based nanolithography, that is, low throughput. Simultaneous generation of multiple patterns scratched into 800 nm thick photoresist and 200 nm thick gold layers has been successfully demonstrated. Scratch marks as narrow and as long as ∼50 and 27 µm, respectively, have been generated in the *X* and *Y* directions using two different microactuator structures carrying 10 and 64 nanotips.

1. Introduction: Within the past few decades, there has been a strong demand for transition from microworld towards smaller sizes to achieve faster, more power efficient, and more powerful integrated electronic and electromechanical devices and systems. Constraints associated with lithography at the nanoscale, however, have been the major obstacles to the mass fabrication of such at the industrial level. In effect, despite the significant progress recently made in the field of nanolithography and nanofabrication, a truly low-cost, high resolution and high throughput approach is yet to be shown. The majority of currently available high-precision nanolithography techniques are based on direct or serial writing, that is, scanning the substrate with a beam of electrons (electron beam lithography (EBL) [1]) or ions (focused ion beam (FIB) [2]) or a nanomechanical probe tip (scanning probe lithography (SPL) [3]). The supporting controllers and readers required in EBL and FIB are generally too bulky and costly to allow parallel processing capability. Whereas, SPL is capable of improving the throughput using a large array of nanomechanical tips. The main difficulty to achieve this goal is, however, to establish uniform contacts between such large arrays and the sample substrates over large areas. Lately, several attempts have been made to overcome the problem by introducing new protocols, for example, polymer pen lithography [4] and hard-tip, soft-spring lithography [5]. Such state-of-the-art probe arrays are then mounted onto custom-made AFM scanners that are equipped with lithography software for generating simultaneous patterns on target substrates. Despite demonstrating promising results over a 1 cm^2 area, having to use sophisticated AFM systems, such techniques are still highly dependent on external readout and actuation apparatus. Instead, probe arrays could be fabricated on relatively large MEMS actuators to eliminate the need for an external nanopositioning system and provide more flexibility [6]. Incorporation of a very large number of MEMS actuators each carrying an array of monolithically integrated nanoprobes could offer a shortcut towards a parallel scanning probe nanolithography at much lower cost [7]. This Letter reports on the parallel generation of multiple submicron patterns using such devices.

2. Device fabrication and description: Monocrystalline silicon microactuators (nanopositioners) with integrated nanotip arrays were fabricated using a combination of frontside and backside micromachining steps performed on a silicon-on-insulator substrate with the device and handle layer thicknesses of 100 and 400 µm, respectively (see Fig. 1). A relatively thick device layer was used to result in robust nanopositioning platforms with minimum out-of-plane motions when actuating the *xy* actuators. A thick layer of low pressure chemical vapour deposition low-stress silicon nitride was first deposited and microscale patterns for generating nanotips were formed (Fig. 1*a*). As shown in Fig. 1*a*, the nitride layer is only etched half way through so that a thicker nitride layer is kept at locations where tips are to be formed. This is immediately followed by two other lithography steps to define the structures as well as backside patterns (Fig. 1*b*). The backside etch was then performed to remove the silicon handle and buried oxide layers underneath the moving parts of the actuator (deep reactive-ion etching (DRIE) and HF dip) (Fig. 1*c*). The opening on the backside allows monitoring of the pattern generation and samples during the operation while eliminating any potential stiction issues. Removing the oxide layer also prevents the formation of notches at the bottom of trenches when doing the Bosch process, using a DRIE tool that is not equipped with a low frequency generator, on the device layer at the next step. After forming the actuators via DRIE of the device layer (Fig. 1*d*), the structures' sidewalls were covered by a 100 nm thermally grown oxide layer (Fig. 1*e*) to protect them during the following isotropic silicon etching step for forming the tips. The nitride layer was then etched back partway, leaving behind only nanotip patterns. The probes were finally formed by isotropic plasma etching of the silicon (Fig. 1*f*).

Figs. 2 and 3 show SEM views of two different structures fabricated using the presented fabrication process. As is shown, thermal actuation is used to attain larger displacements at lower actuation voltages compared to the electrostatic actuation mechanism. Each structure employs two sets of similar electrothermal bent-beam actuators, also called chevron, providing displacements in two-degrees-of-freedom (2DOF). Each chevron actuator is comprised of a pair of inclined beams and the point in which the two inclined beams intersect is linked to a central platform that carries an array of nanotips. Such a configuration is used to cover the maximum displacements at the tip locations when scanning the surfaces. For structure 1 (S1), 64 probes are integrated on a single moving stage that undergoes almost spinless *xy* movements because of its symmetrical arrangement. Any possible difference in the height of the probes in S1 makes it challenging to establish uniform contacts between the sample substrate and every single

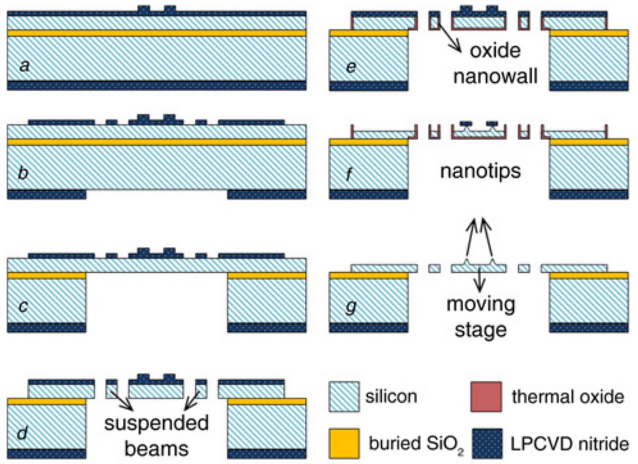

Figure 1 *Schematic side-view of the process flow used for fabrication of the MEMS positioning systems integrated with nanotips*
a A thick LPCVD nitride layer deposition followed by generation of the nanotip patterns (etched half way)
b Defining the structure as well as the backside patterns
c Backside etch using DRIE to remove the handle and buried oxide layers
d Forming the structures via DRIE of the device layer
e Growing a 100 nm thick thermal oxide for sidewalls protection
f Partly etching back the front-side nitride mask followed by isotropic dry etch of silicon to form the tips
g Dipping the sample in hydrofluoric acid for removing the oxide

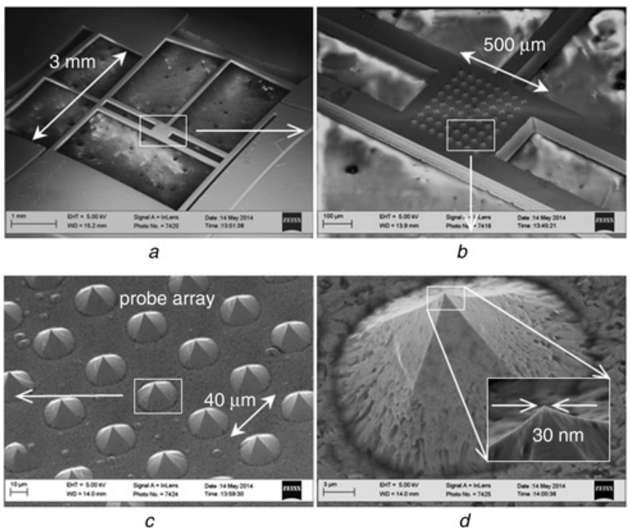

Figure 2 *SEM view of one of the fabricated structures (S1) (Fig. 2a); moving platform carrying 64 nanotips (Fig. 2b); array of nanotips (Fig. 2c); single probe with tip as sharp as 30 nm (Fig. 2d)*

probe. Whereas, structure 2 is equipped with a smaller number of probes (10 nanotips) each embedded on individual cantilevers. Even though S2 cannot provide fully spinless movements, it is capable of providing vertical control over individual nanotips and in turn uniform contact between the sample substrate and the probe array.

Unlike electrostatic positioning systems, in which one actuator can be easily deployed on the frame that moves along the other actuator, it is somewhat difficult to completely eliminate the mechanical crosstalk between the *x* and *y* actuators when it comes to thermal actuation. The comparatively longer linkage beam, connected to the central stage, used for the *y*-actuator is to alleviate such crosstalks as well as the extra stiffness introduced by that linkage in the perpendicular direction. Long wirebond pads were

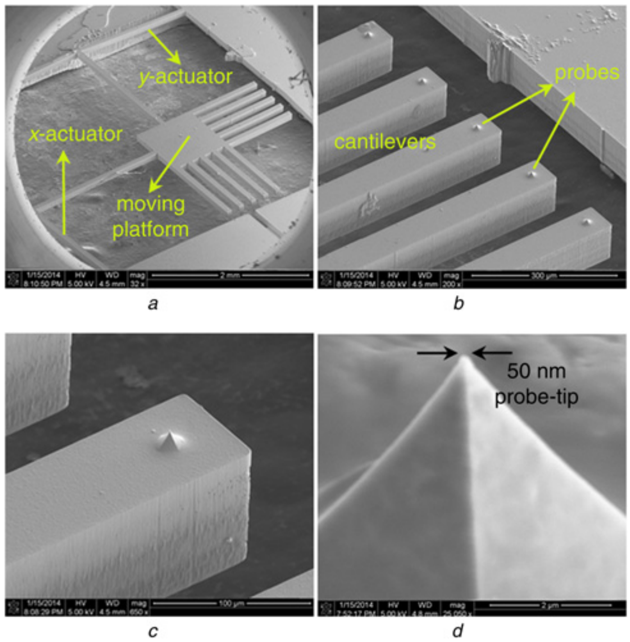

Figure 3 *SEM view of another fabricated structure (S2) (Fig. 3a); array of cantilevers functioning as moving platforms (Fig. 3b); single cantilever carrying one probe (Fig. 3c); 30 nm sharp probe-tip (Fig. 3d)*

incorporated in the actuator layouts to have sufficient room for placing the sample substrate in contact with the moving platform without running into wirebonds.

3. Results and discussion: To perform the tests, the actuator chips were placed in the designated location on the specifically designed PCB and wire bonded to the metal tracks on the PCB using aluminium wires. The relatively large opening drilled in the PCB is to visually inspect the device performance and pattern generation while the sample substrate is placed on the device. Silicon chips coated with 800 nm thick photoresist as well as a 200 nm gold (Au) layer evaporated on the photoresist were used as target substrates. The sample substrates were brought into contact with the MEMS chips, using a *z*-axis micropositioning system, engaging the probes with the substrate. The device operation was then monitored with an inverted microscope (see Fig. 4). Voltage–displacement characteristics of the actuators of S1, measured using a high magnification optical microscope, are

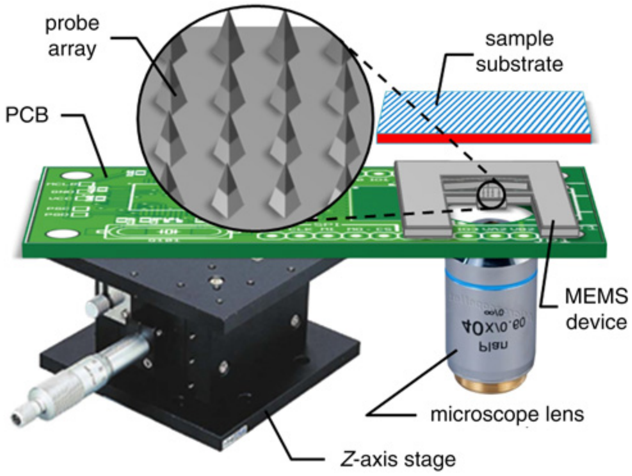

Figure 4 *Schematic view of experimental setup*

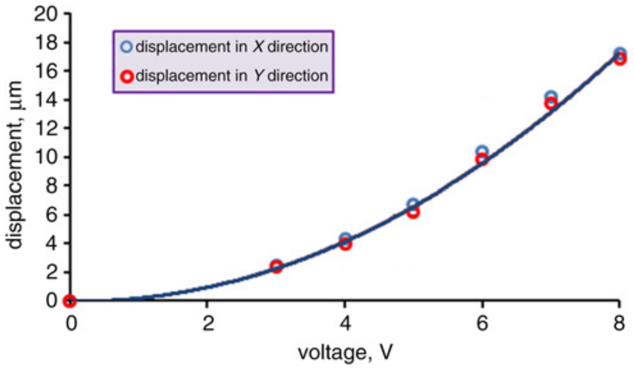

Figure 5 *Voltage–displacement characteristics of xy electrothermal actuators as a function of the differential input voltage, measured while other actuator is kept at rest*

shown in Fig. 5. The displacement of each actuator is recorded while keeping the adjacent actuator at rest, showing almost similar performance for the two as a result of the same input voltages. Applying different combinations of voltages to the two perpendicular actuators of S1, different multiple quadrilateral patterns (as long as ∼16 µm) with 40 µm pitches were generated (Fig. 6). Despite efforts to minimise the coupling between the x and y actuators, the imperfect straight lines are caused by the electrical crosstalk because of the structure being fully monolithic and conductive. As discussed earlier, different probe heights in S1 does not allow some probes to establish contact with the sample substrate. To address this issue, structure S2 with nanotips located on separate cantilever beams coupled to the central moving platform was also fabricated and tested; however, this resulted in a larger pitch size of 200 µm. Figs. 5*a* and *b* illustrate SEM views of scratches generated by S2 on an 800 nm photoresist layer and by S1 on a 200 nm Au layer evaporated on photoresist, respectively. Being a more compliant structure, S2 resulted in scratches twice as long as those attained by S1. By adjusting the loading force, that is, elevation, of the tips towards the sample substrate, trenches with different depths/widths, as narrow as 50 nm at the bottom of the trenches, have been demonstrated.

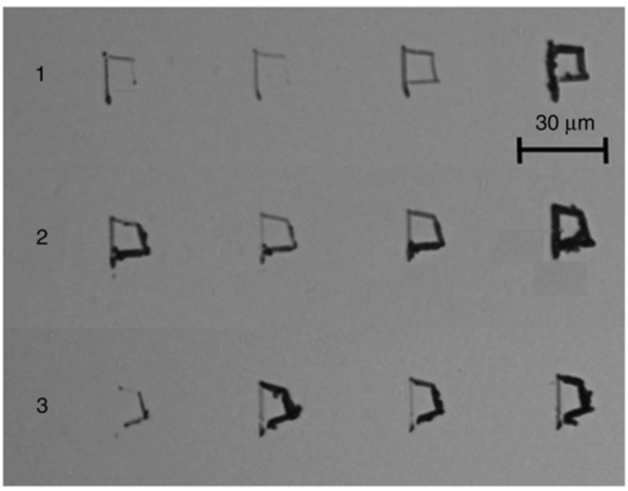

Figure 6 *Different patterns generated by applying different combinations of voltages to the two perpendicular actuators of S1*

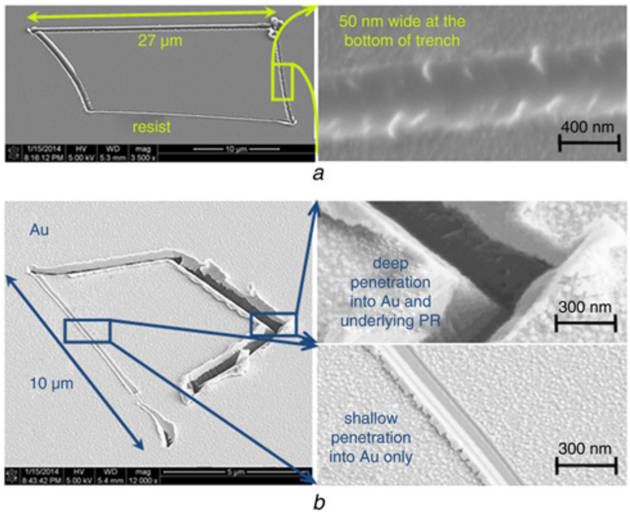

Figure 7 *SEM view of patterns generated on 800 nm thick photoresist by S2 (Fig. 7a), and 200 nm thick Au by S1 (Fig. 7b)*

4. Conclusions and future work: Preliminary results on the simultaneous generation of multiple nanoscale features, as narrow as 50 nm, have been demonstrated using MEMS actuators with two-dimensional arrays of monolithically integrated nanoprobes. The presented technique is potentially a new enabling technology for low-cost high throughput parallel scanning probe nanolithography. Different configurations of 2DOF electrothermal actuators were successfully fabricated, tested and evaluated as scanning surface profilers, showing displacements as long as 27 µm. Owing to the electrical and mechanical crosstalks between the x and y actuators, it was not possible to generate arbitrary patterns at this point. In the next generation of the devices, such crosstalks will be eliminated, leading to fully decoupled structures, both mechanically and electrically. Demonstrating large arrays of nanowires using such devices will also be performed using the same method.

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6 References

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