Electronically Temperature Compensated Silicon Bulk Acoustic Resonator Reference Oscillators

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***Abstract*—The paper describes the design and implementation of an electronically temperature compensated reference oscillator based on capacitive silicon micromechanical resonators. The design of a 5.5-MHz silicon bulk acoustic resonator has been optimized to offer high quality factor (>100 000) while maintaining tunability in excess of 3000 ppm for fine-tuning and temperature compensation. Oscillations are sustained with a CMOS amplifier. When interfaced with the temperature compensating bias circuit, the oscillator exhibits a frequency drift of 39 ppm over 100 °C as compared to an uncompensated frequency drift of 2830 ppm over the same range. The sustaining amplifier and compensation circuitry were fabricated in a 2P3M 0.6-μm CMOS process.**

***Index Terms*—Reference oscillators, MEMS resonators, MEMS oscillators and temperature compensation.**

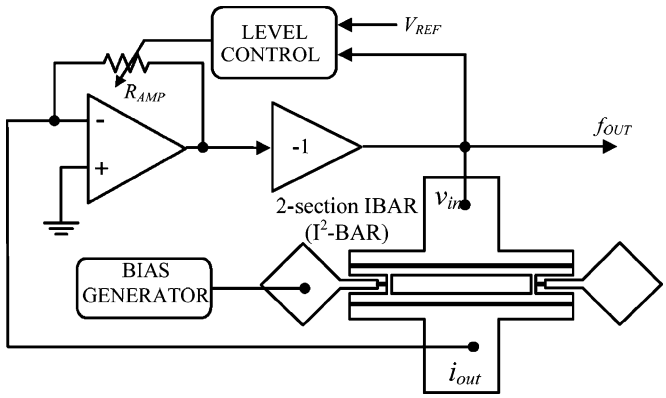

Fig. 1. Block diagram of the Reference Oscillator.

I. Introduction

THE reference oscillator is usually one of the hardest blocks in a system to integrate on silicon. While quartz crystals offer excellent temperature stability and phase noise performance, the incompatibility with silicon integration increases the size of systems that rely on clocking schemes. Silicon micromechanical resonators have been proven to offer excellent stability and quality factors in excess of 50 000 over a wide range of frequencies [1]–[3] making them suitable for reference oscillators. The potential for electrostatic tuning of these resonators without using noisy varactor diodes is an attractive option for electronic fine tuning and temperature compensation of the resonant frequency. Further, these devices also offer the possibility of integration at the chip or package level with standard CMOS electronics.

While micromechanical resonators have been proven to offer excellent quality factors, the uncompensated temperature stability of these resonators (typically about -26 ppm/°C for the single crystal silicon resonators discussed here) [2] is far inferior to that of quartz. Conventional resonator temperature compensation schemes focus on localized resonator heating or stress compensation techniques [4]–[6]. The idea of electrostatic compensation is largely unexploited due to the need for large voltages, conventionally unavailable in CMOS.

In this work, we demonstrate a technique for electrostatic temperature compensation of a silicon bulk acoustic resonator-oscillator with standard CMOS electronics operating with a 5-V supply. The idea of electrostatic temperature compensation is first introduced. With an optimal design of the I-shaped bulk acoustic resonator (IBAR), we have achieved exceptionally high Q and improved frequency tunability. Standard voltage multiplication techniques [7] are adapted to yield voltages in the range of 25 V with an appropriate temperature coefficient. Frequency stability of 0.39 ppm/°C over a 100 °C temperature range is demonstrated with the compensating scheme, a 72X improvement over an uncompensated oscillator and an 8X improvement over a previously reported scheme [8]. Performance limits of the compensating technique are identified and the techniques to improve performance are suggested.

II. System Block Diagram

Fig. 1 shows the complete system block diagram of the implemented resonator oscillator system. The oscillation frequency is determined by a high-Q micromechanical resonator. Oscillations are started up and sustained with the amplifier and inverting buffer that maintain unity loop gain and zero phase shift. The gain of the amplifier is varied with a voltage-controlled MOS resistor (controlled by an automatic level control circuit) to minimize resonator saturation due to large drive amplitudes. The resonator is biased with a voltage in the range of 25 V (with an appropriate negative temperature coefficient) generated from

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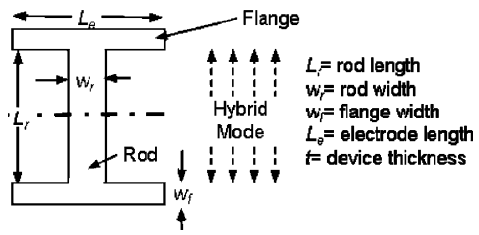

Fig. 2. Design of a 5.5-MHz extensional mode resonator for low impedance and high tunability.

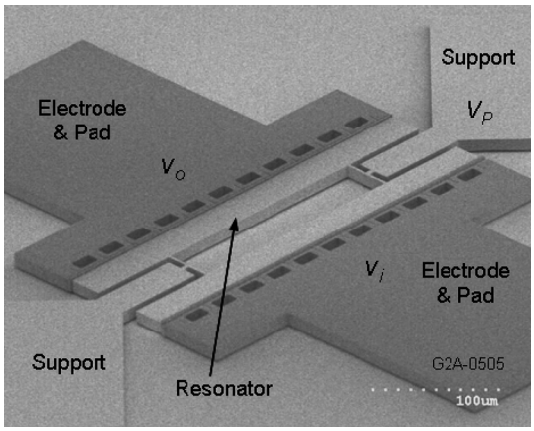

Fig. 3. SEM picture of IBAR used in this work.

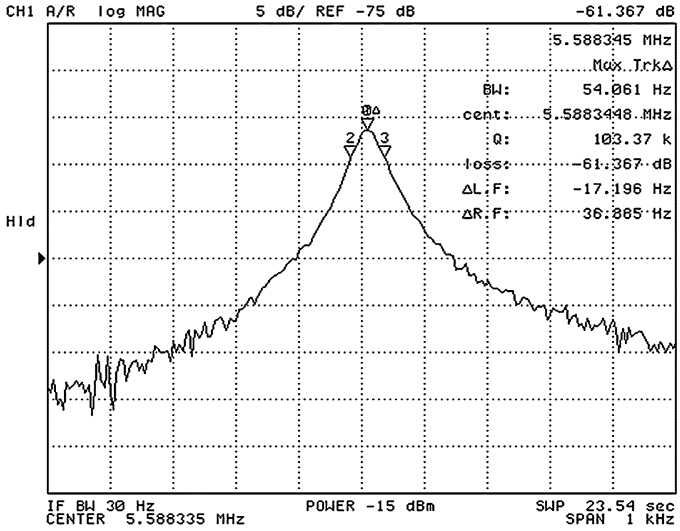

Fig. 4. Open-loop frequency response of the IBAR at 3-V bias; $f = 5.59$ MHz; $Q = 103\,370$.

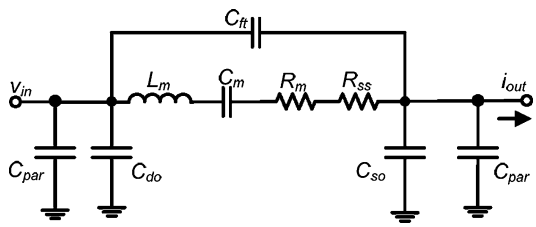

Fig. 5. Electrical equivalent circuit of the 5.5-MHz I^2-BAR at 10-V bias ($L_m = 15.4$ H, $C_m = 52.8$ aF, $R_m = 10$ kΩ, $C_{\rm par} = 2$ pF, $R_{\rm ss} = 3.5$ kΩ).

a charge pump based biasing circuit. The clock ripple on the bias voltage is minimized by using a low-pass ripple filter at the output of the charge pump.

III. Micromechanical Silicon Resonator Design

The characteristics of the resonator are dictated by the system-level requirements: to achieve low phase noise, low power consumption, and reduced frequency–temperature drift, the micromechanical resonator must have high quality factor, low motional impedance, and high tunability for electrostatic frequency tuning.

These three requirements are typically difficult to achieve simultaneously with a micromechanical resonator. Flexural mode capacitive beam resonators in the frequency of interest are highly tunable, but have high impedances and lower Q (<50 000). Conventional extensional mode capacitive resonators can have high Q (>100 000) and lower impedances, but suffer from low tunability. Piezoelectric resonators are another alternative; they have lower impedances, but no effective tuning technique has been demonstrated for these resonators.

The new I^2 bulk acoustic resonator (I^2-BAR) was designed to meet all the above requirements simultaneously [9]. The I-shaped bulk acoustic resonator (IBAR) is presented as the solution (Figs. 2 and 3), although semantically, its mode is not present in the bulk. The hybrid structure is a combination of a flexural component (flange) and an extensional member (rod). In the desired mode, the flange provides large area and low stiffness for good electrostatic tuning and low motional resistance (R_m), and the symmetric extensional nature provides high Q. The ability to combine multiple sections for greater transduction area further reduces R_m. The device shown in the SEM of Fig. 3 is a two-section IBAR, otherwise known as an I^2. The structure resonates predominantly in a lateral extensional mode. Large flanges are placed at the ends of the extensional beams for increasing the capacitive transduction area (Fig. 2). While a detailed discussion of the design is beyond the scope of the paper, it may be stated that an optimal design of the flange and the rod can achieve the desired properties of high quality factor and tuning. The resonator, which is fabricated using the HARPSS-on-SOI process [2], is shown in Fig. 3. The resonator in Fig. 3 had a resonant frequency of 5.58 MHz with a Q of 103 000. The frequency response is shown in Fig. 4.

The resonator is modeled electrically as a series *R-L-C* tank circuit shown in Fig. 5. The parasitic capacitances to ground include the device electrode to substrate capacitance in parallel with the static capacitance. The feed-through from input to output is modeled as a capacitance in parallel with the tank. The motional impedance, which represents the loss component of the resonator, was measured to be approximately 10 kΩ with a polarization voltage of 10 V. A series resistance $R_{\rm ss}$ is included to model the body resistance of the resonator which loads the quality factor of the device at higher bias voltages. While the added series resistance does decrease the quality factor, it offers an advantage in that the device impedance is no longer a strong function of the bias voltage. This allows us to change the frequency with the bias voltage (for temperature compensation)

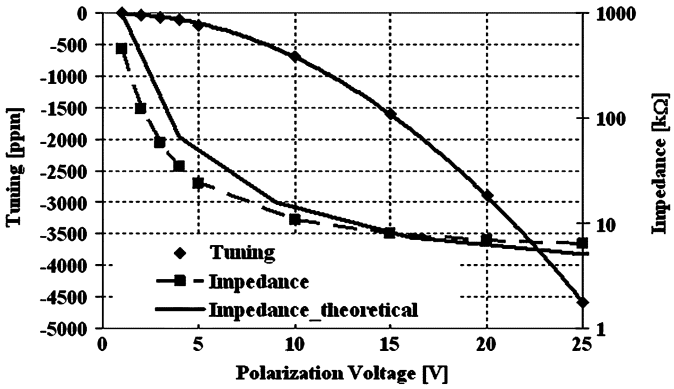

Fig. 6. Measured impedance and tuning characteristic of the 5.5-MHz I^2-BAR. $R_0 = 10$ kΩ at 10-V bias. Tuning = 4600 ppm from 2–25 V.

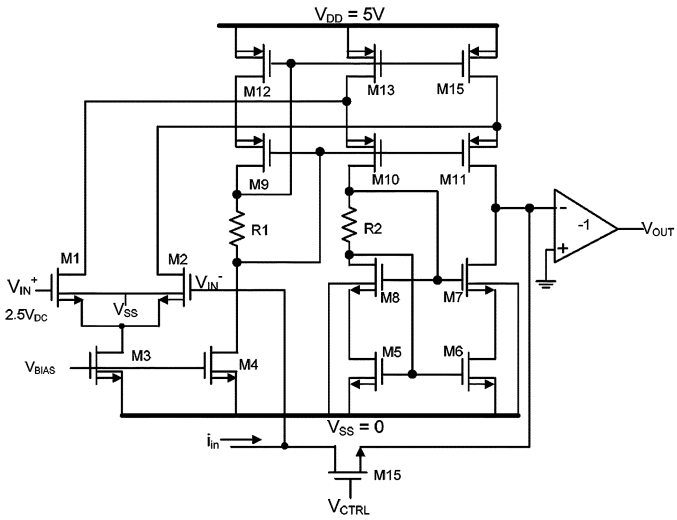

Fig. 7. Schematic diagram of sustaining transimpedance amplifier showing MOS resistor M15.

without changing the transimpedance gain with the automatic level control (ALC) circuit by a large factor (>10).

The temperature variation of the resonant frequency can be approximated as a linear relation as expressed in (1), as a result of the temperature coefficient of the Young's modulus of silicon and that of thermal expansion [9].

$$\left(\frac{\Delta f}{f_0}\right)_T \approx \gamma_T (T - T_0) \tag{1}$$

where γ_T is the temperature coefficient of the resonant frequency. The frequency tuning characteristic with V_P is proportional to V_P^2 and is given by (2) [8].

$$\frac{\Delta f}{f_0} = -\frac{\varepsilon A f_0 \left(V_P^2 - V_{P0}^2\right)}{k_n d_o^3} \tag{2}$$

where A is the area of the electrode, d_0 is the electrode gap, f_0 is the natural frequency of the resonating structure (with zero V_P), Δf is the difference between the measured frequency f_0 (at a bias voltage of V_{P0}) and the operating frequency (at the operating V_P), and k_n is the stiffness of the resonator. The measured impedance and tuning characteristic of the device with bias voltage are shown in Fig. 6.

IV. Interface Circuit Architectures

A. Sustaining Amplifier

The sustaining amplifier for the oscillator is based on a CMOS transimpedance amplifier with a self-biased folded-cascode operational transconductance amplifier (OTA) as the core. The schematic of the sustaining amplifier is shown in Fig. 7. An inverting buffer is used at the output of the amplifier to drive an off-chip load and also to maintain zero loop phase shift. The amplifier is implemented in a shunt–shunt feedback configuration to minimize Q-loading [10].

B. Automatic Level Control

To maintain optimal phase noise performance, it is essential to control the drive amplitude of the resonator to minimize nonlinearity in the resonator [11]. In crystal oscillators, amplitude limiting typically occurs due to the nonlinearity of the transistors in the amplifier. However, quite often with micromechanical resonators, the resonator is driven into the nonlinear region at smaller signal amplitudes, when the circuit is still within its linear operating region. This can occur as a result of geometric, material, or transduction nonlinearities in the resonator.

Hence, it is essential to limit oscillation amplitude to values smaller than the distortion limit set by the amplifier. This is achieved with an ALC circuit, shown in Fig. 8. Level control is achieved by detecting the output signal amplitude using a peak detector, comparing the amplitude to a threshold value $V_{\rm ALC}$ (that depends on the type of resonator used—about 10 mV in this case), and generating an error voltage to control the gate of the MOS resistor M15. This varies the transimpedance gain of the sustaining amplifier (Fig. 7), thus limiting the oscillation amplitude within the linear limit of the resonator.

C. Temperature Compensating Bias Circuitry

As discussed earlier, the temperature drift of the resonator is linear and approximately −26 ppm/°C for the resonators discussed here. As we can observe from Fig. 6, the frequency also decreases with an increase in the polarization voltage. So, if the polarization voltage has appropriate negative temperature dependence, the change in frequency with temperature is offset by a change due to the polarization voltage. The first version of such a compensating bias generator was designed and reported earlier [8] and uses a DC charge pump in conjunction with a chain of diodes to generate a linear temperature slope for the bias voltage. It has been established that perfect linear compensation can result in temperature stability no better than 200 ppm [9]. Although this is a significant improvement over an uncompensated oscillator, this number is still poorer than typical quartz.

The above-mentioned technique is limited in applicability to resonators within a narrow tuning range, due to the fairly constant temperature coefficient of $V_{\rm BE}$. Further, it may be observed from (1) and (2) that the frequency tuning is a parabolic function

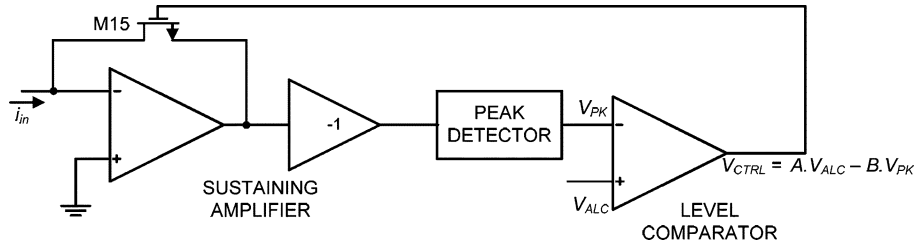

Fig. 8. Block diagram of automatic level control (ALC) circuit.

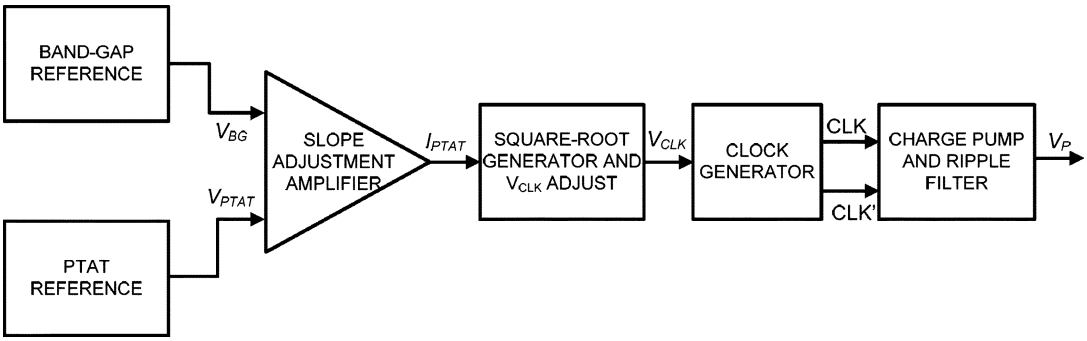

Fig. 9. Block diagram of parabolic temperature compensating bias generator (TCB) circuit.

of V_P and a linear function of temperature. Hence, to achieve a zero temperature coefficient oscillator, one should have

$$\left(\frac{\Delta f}{f_0}\right)_T = -\left(\frac{\Delta f}{f_0}\right)_V. \tag{3}$$

Hence, the polarization voltage should vary with temperature as a parabolic function given by (4).

$$V_P^2 = -\frac{\alpha_T k_n d_0^3}{\varepsilon A f_0}(T - T_0) + V_{P0}^2 = A - B(T - T_0). \tag{4}$$

The block diagram of a circuit that can generate a voltage of the form of (4) for accurate temperature compensation is shown in Fig. 9.

The bandgap and the proportional to absolute temperature (PTAT) reference circuit generate a constant voltage and a linear temperature slope, respectively. These voltages are scaled using amplifiers to generate a voltage function of the form of (5). A block diagram of the slope adjustment amplifier itself is shown in Fig. 10. Two low-power opamps are used at the first stage to scale the bandgap and the PTAT voltages by the gain coefficients A_1 and B_1 by using an appropriate resistance ratio to set the closed-loop gain. On the test chip, these coefficients were set on the test board with off-chip resistors. In a manufacturing environment, the coefficients A_1 and B_1 can be trimmed by trimming two resistors to achieve the desired temperature stability specification. This may be in addition to any trimming that may be performed on the bandgap resistors to trim the temperature coefficient (TC) of the bandgap circuit. A differential transconductance stage then combines the difference voltages to generate the required PTAT current $I_{\rm PTAT}$.

$$V_X = A_1 - B_1 T. \tag{5}$$

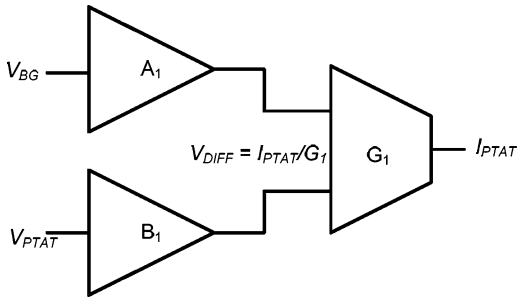

Fig. 10. Block diagram of slope adjustment amplifier in bias (TCB) generator.

V_X is used to generate a PTAT current $I_{\rm PTAT}$, the square root of which is taken and used as a power supply for a clock generator. The generated clock thus swings between 0 and $V_{\rm CLK}$, where $V_{\rm CLK}$ is of the form of (6).

$$V_{\rm CLK} = K\sqrt{A_1 - B_1 T} \tag{6}$$

where K is the scaling coefficient of the transconductance stage.

This voltage is multiplied by a charge pump to yield a large DC voltage of the form of (7). Equation (7) contains a diode loss term which affects the value and the temperature slope of the generated voltage. This can be offset by adding an offset voltage equal to the loss term at the last stage.

$$V_P \approx N \cdot (\sqrt{A_1 - B_1 T} - V_{\rm diode}). \tag{7}$$

The circuits used for each of the blocks above are described in the following section.

1) Band-Gap and PTAT Generator: The bandgap circuit used in the implementation is shown in Fig. 11. The circuit is based on a textbook architecture [13] that uses the summation of complementary to absolute temperature (CTAT) voltage (generated by the $V_{\rm BE}$ of a bipolar transistor) and a PTAT

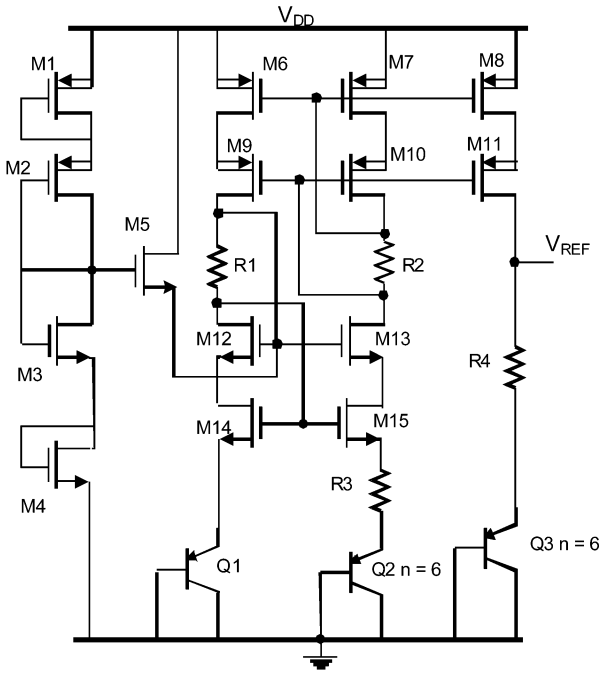

Fig. 11. Schematic of bandgap and PTAT generator. BG and PTAT voltages are obtained by choosing different values for the diode sizes (ratio "*n*") and different resistor sizes (R4/R3).

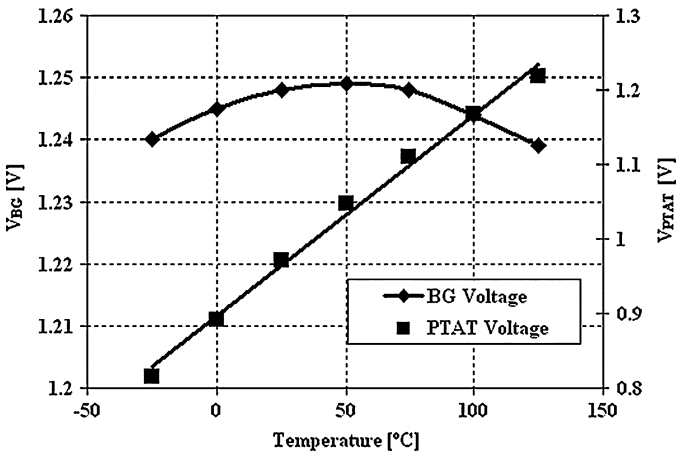

Fig. 12. Generated bandgap and PTAT voltages versus temperature.

voltage (generated by the ΔV_{BE} between two such devices). The PTAT circuit is generated by a similar architecture by simply changing the resistor ratio. The measured temperature behavior of the bandgap and the PTAT circuits is shown in Fig. 11.

The temperature coefficient of the bandgap cell is approximately 40 ppm/°C. The temperature slope of the PTAT circuit is about 3 mV/°C. The curvature of the bandgap and the PTAT voltage is evident from Fig. 12; the curvature sets a limit on the accuracy of the generated clock voltage and hence the compensating bias voltage.

2) Square-Root Generator: The circuit schematic of the square-root generation circuit is shown in Fig. 13 and is a derivative of the circuit discussed in [14]. The analysis of the

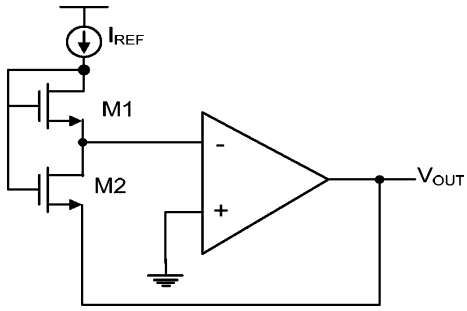

Fig. 13. Square-root generation circuit schematic.

circuit is found in [14]. Writing the current equations for M1 and M2 and simplifying, we get

$$V_{\rm OUT} \approx \sqrt{2I_{\rm REF}}\,\lfloor\sqrt{(1/K_1)+(1/K_2)} - \sqrt{(1/K_2)}\rfloor. \quad (8)$$

If the transistors are sized equal, then the transconductances $K_2 = K_1 = K$ and the expression for $V_{\rm OUT}$ can be simplified as

$$V_{\rm OUT} = \frac{(2-\sqrt{2})}{\sqrt{K}}\sqrt{I_{\rm REF}}. \quad (9)$$

Thus, the output voltage of the circuit is proportional to the square root of the reference current. In (8), the body effect of M1 cannot be ignored and will affect the linearity of the circuit. However, this effect can be minimized by sizing the transistors appropriately. Now, if the reference current is generated as a function of the bandgap and PTAT voltages, then we can get an output voltage that is of the form of (6). Hence, the amplifier used to generate the function $(A_1 - B_1 T)$ from the bandgap and the PTAT generators is a transconductance stage rather than a voltage amplifier.

The square-root generator has a "gain" error because of the change in mobility with temperature. However, the gain of the transconductance stage used to generate $I_{\rm REF}$ is also made proportional to g_m. Thus, as long as the gain of the transconductance stage and the gain of the square-root generator depend on the g_m of the same type of device biased appropriately, the temperature effects will cancel out to the first order. In this case the transistors were similarly sized nMOS devices biased above threshold and in saturation.

3) Charge Pump and Clock Generation: The clock generator and the charge pump used in the last two stages of the compensation circuit are the same as the ones used for the linear compensation circuit [8]. A standard Dickson pump architecture is used for the charge pump since the voltage across the diodes is never greater than $V_{\rm DD}$ in this scheme as compared to voltage doubler type charge pumps [12] that offer higher efficiency. The circuit diagram is shown in Fig. 14. The diodes were made using the p+-n-well junction in the process. The maximum voltage that can be generated is determined by two factors: the leakage and ultimate breakdown of the n-well substrate junction and the breakdown of the poly–poly capacitor. The clocks for the charge pump are realized on the chip using an inverter delay ring oscillator and a logic circuit to generate nonoverlapping clocks. The logic diagram for the clock generator is given in Fig. 15.

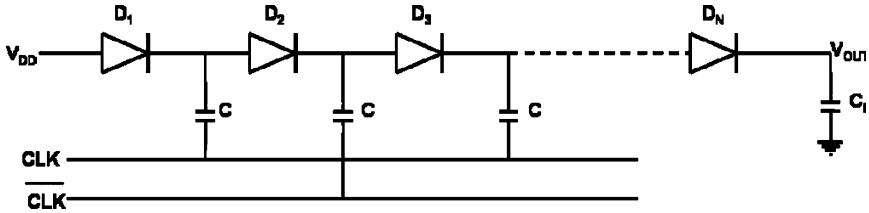

Fig. 14. Square-root generation circuit schematic.

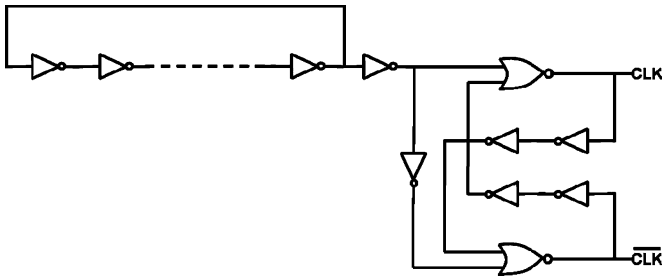

Fig. 15. Logic diagram of nonoverlapping clock generator.

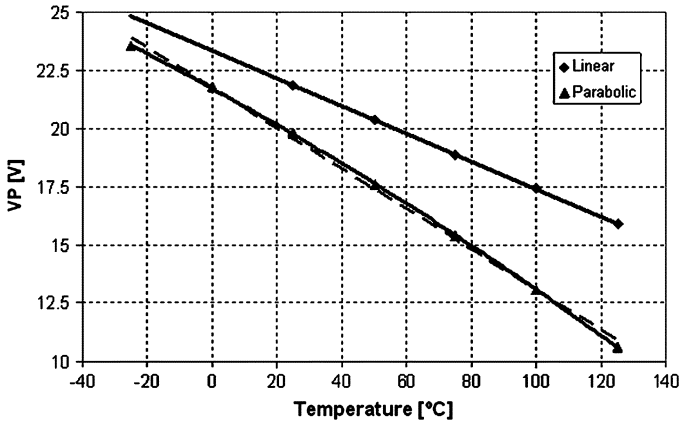

Fig. 16. Generated polarization voltage versus temperature for linear and parabolic compensation circuits.

In the parabolic compensation technique, the charge pump temperature coefficient adds a linear temperature dependency to the parabolic function represented by (7) and needs to be accounted for. This is accomplished by adjusting the coefficients A_1 and B_1 to account for the dependency or by adding the loss term equal to $N \cdot V_{\mathrm{diode}}$ to the final stage capacitor. In this case, the former approach is chosen.

4) Comparison of Linear and Parabolic TCB Circuits: The voltage generated (measured) from the linear and parabolic compensation circuits is shown in Fig. 16 as a function of temperature. A linear fit is also shown for the parabolic voltage case to highlight the curvature arising from the quadratic term. It may be noted the values of V_P shown in Fig. 16 for the parabolic compensation circuit are slightly different from the values used while performing temperature compensation since the coefficients A_1 and B_1 were adjusted to account for the temperature coefficient of the charge pump diodes after characterization.

The difference between the linear and parabolic compensation voltages is evident from Fig. 16, although the curvature of the parabolic voltage is quite small. In fact, a linear approximation of the same results in less than 5% error (200 mV over 25 V). However, the 200 mV error still degrades temperature stability to the extent of 250 ppm.

It may be observed that the parabolic compensation circuit adds significantly to circuit complexity due to the inclusion of the bandgap and PTAT generators, the square-root generators and a number of scaling amplifiers. However, this does not result in significantly higher power consumption. This is because the bandgap and the PTAT generators and the associated amplifiers can be operated at very low current levels (less than 2 μA for all the blocks). The amplifier at the last stage of the square-root generation block is used to generate the supply voltage for the clock generator and hence has to drive a large current. Hence, this block consumes about 170 μA of current. But generating an internal clock supply voltage also means that the clock generator does not draw current directly from the supply. Hence, the increase in power consumption due to the added circuitry is less than 100 μW.

V. Measured Results

The interface IC was fabricated in a two-poly three-metal (2P3M) 0.5-μm CMOS process. The gain–bandwidth (GBW) of the opamp was measured to be 175 MHz, which is large enough to satisfy the gain requirements to sustain oscillations. The temperature behavior of the bandgap and PTAT generators was verified (Fig. 12) and the temperature coefficient was computed.

1) Oscillator Phase Noise: After open-loop characterization, the resonator and the IC were interfaced with bond wires and tested under a vacuum probe station to verify the functionality of the oscillator. The phase noise of a 5.5-MHz oscillator (open-loop Q of 103 000, $V_P = 3$ V) was measured using an Agilent E5500 phase noise analyzer (Fig. 17). A smaller value of polarization voltage was chosen deliberately for two purposes: the motional impedance is higher and that minimizes Q-loading and improves near-carrier phase noise performance; and a smaller polarization voltage allows for larger signal amplitude while maintaining the resonator in its linear operating region, thus improving phase noise performance both near and far from carrier. This, however, comes at the cost of additional power consumption in the loop amplifier, since the GBW requirement for the transimpedance amplifier is higher.

The near-carrier phase noise at 10 Hz offset was measured to be approximately -66 dBc/Hz and at an offset of 1 kHz is about -112 dBc/Hz. The phase noise floor far from carrier is at -135 dBc/Hz. This is largely a result of the noise floor of the interface amplifier and the operating power level of the oscillator, which was about -10 dBm. The phase noise floor is close to the

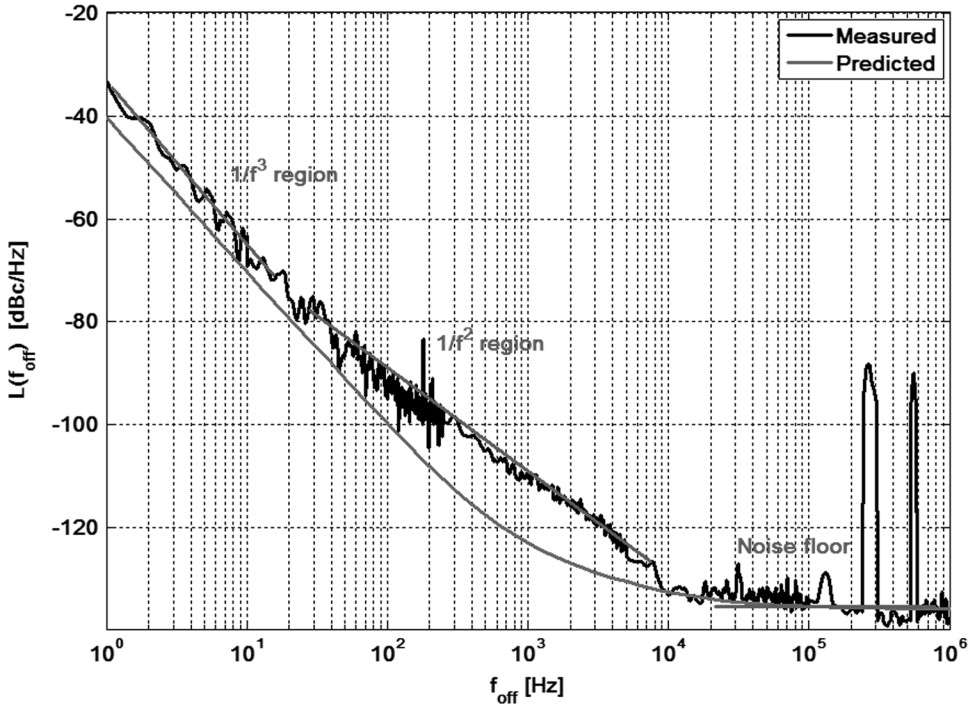

Fig. 17. Phase noise of the 5.5-MHz oscillator.

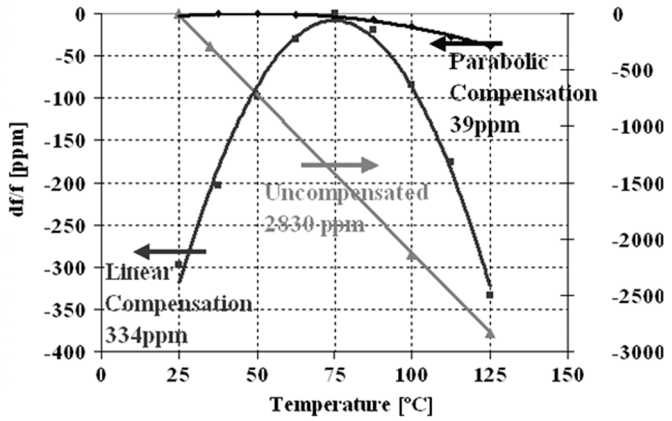

Fig. 18. Comparison of temperature stability of the oscillator with linear and parabolic compensation and w/o compensation.

number predicted by the power handling of the resonator (about −10 dBm) and the noise of the amplifier. However, despite the high-Q of the resonator, a strong $1/f^2$ noise component is present in the phase noise spectrum. This can be attributed to the noise introduced by the bias generator which can be shown to add further to the $1/f^2$ noise [15]. Most of the noise is actually from the resistors used to set the tuning coefficients and the noise of the bandgap and PTAT generators and the low power amplifiers in the chain. It may be noted that no charge pump was used in this experiment and hence no clock ripple is observed on the spectrum. The error in the predicted 1/f noise is largely attributed to the lack of certainty in the flicker noise numbers for the process. The noise floor in this case is determined by the power handling limit of the resonator which was about −10 dBm. As expected, the $1/f^4$ and $1/f^3$ regions are present very close to carrier. The predicted $1/f^3$ corner noise also includes coefficients for resonator and transistor nonlinearity and is determined from resonator characterization. While the phase noise characteristic at the temperature compensating bias voltage is most useful, it may be noted that the phase noise is expected to deteriorate due to the smaller power handling limit and additional charge pump bias generator noise at higher bias voltages. The lack of sensitivity of the ALC circuit to small operating voltages (below 10 mV) prevents us from effectively limiting nonlinearity in the resonator and hence an accurate determination of the phase noise at the voltages. Nevertheless, given that the power handling ($\mathrm{P_{in}}$) and quality factor of the devices described here at the temperature compensating bias voltages (at 16-V bias, $\mathrm{Q} = 35\,000$ and $\mathrm{P_{in}} = -30$ dBm at 16 V) far exceeds that of beam resonators [4], the phase noise can be expected to be about 10 dB better than the beam counterparts even accounting for the additional bias voltage induced noise.

2) Temperature Stability: To evaluate the temperature stability of the oscillator, the sample was placed in a vacuum chamber with temperature control. The results obtained from the linear temperature compensation circuit have been reported earlier for a 4-MHz oscillator [8]. After characterizing the functionality of the bandgap and PTAT generators (temperature behavior shown in Fig. 12) and the square-root generator, the temperature coefficient of the charge pumps was characterized. The uncompensated temperature variation is characterized (V_P of 15 V; Fig. 18). Based on the temperature and the tuning coefficients of the device (shown in Fig. 6), appropriate values were chosen for the scaling coefficients A_1 and B_1 (by using a resistor ratio for setting the gain of each amplifier in the chain) and the circuits were connected with bond wires.

The output of the square-root generator was used as the supply to the charge pump clock generator and the oscillator

was biased with the polarization voltage generated from the bias generator. Two test runs were performed: one with the linear compensation circuit and another with the parabolic compensation circuit. The temperature variation of the compensated oscillator was measured to be 332 ppm and 38.7 ppm over a temperature range of 25 °C to 125 °C with the linear and parabolic compensation circuits, respectively. This represents an improvement of 8.5X and 72X over the linearly compensated and uncompensated oscillator, respectively. All temperature stability plots are shown in Fig. 18. It may be noted that all testing was done on unpackaged devices that were bonded to the IC on a custom test board. Since the measurements were made at steady-state and the MEMS device is fabricated on a low resistivity substrate, any temperature mismatch between the MEMS die and the IC is expected to be minimal and so is the error in temperature compensation. Further, since the devices were unpackaged, any thermal mismatch between the IC and the package is unaccounted. However, the effect of package–die TC mismatch may be accounted for easily by adjusting the coefficients A_1 and B_1.

It is interesting to note that for the parabolic compensation case, the zero temperature coefficient point is approximately 50 °C. This indicates that the compensation is suboptimal. This can be a result of an inaccurate choice of the coefficients in generating the V_{CLK} or the nonlinearity of the square-root generation block. The former is quite likely since the choice of the coefficients is based on the exact tuning slope and the temperature coefficient extracted from resonator characterization. The choice of coefficients also needs to account for the temperature slope of the charge pump diodes. For the 5.5 MHz resonator, the temperature coefficient was about -28.3 ppm/°C and the tuning slope was estimated as -7.3 ppm/V^2. A small error in either of these values would result in a wrong choice for the voltage scaling coefficients A_1 and B_1, thus leading to suboptimal temperature compensation. It may be noted from Fig. 6 that the variation of impedance across the tuning voltage range was only a factor of 2 (due to the effect of series resistive loading). Hence, there is no serious degradation of phase noise performance across this range and the MOS resistor M15 can easily track this variation to sustain oscillations across the entire range. The loaded quality factor of the device is measured to be about 30 000 over the temperature compensation range.

A summary of the measured results from the linear and parabolic compensation circuits is given in Table 1. The overall power consumption was about 1.9 mW for the parabolic compensation IC as compared to 1.8 mW for the IC with linear compensation. A die picture of the IC that includes the parabolic compensation scheme is shown in Fig. 19. The overall die area was 1.5 mm $\times$ 1.5 mm. The IC was fabricated in a 2P3M 0.5-μm CMOS process through AMI Semiconductor.

TABLE I
SUMMARY OF SPECIFICATIONS OF REFERENCE OSCILLATOR

Specification	Performance
Resonator Specifications	
Open loop quality factor	
1V bias	112000
3V bias	103000
10V bias	54000
Tuning coefficient	-7.34ppm/V^2
Circuit Specifications	
Amplifier Gain Bandwidth product	175 MHz
Charge pump clock	1 MHz
Ripple filter -3dB frequency	1 kHz
Total power consumption	
With linear compensation	1.8 mW
With parabolic compensation	1.9mW
Die area (for either IC)	2.25mm^2
Oscillator Specifications	
Temperature stability over 100ºC	
Uncompensated variation	-28.3ppm/ºC
w/ Linear compensation	**3.3ppm/ºC**
w/ Parabolic compensation	**0.39ppm/ºC**
Phase Noise performance	
10Hz offset	-66dBc/Hz
100Hz offset	-92dBc/Hz
1kHz offset	-112dBc/Hz
Phase Noise floor	-135dBc/Hz

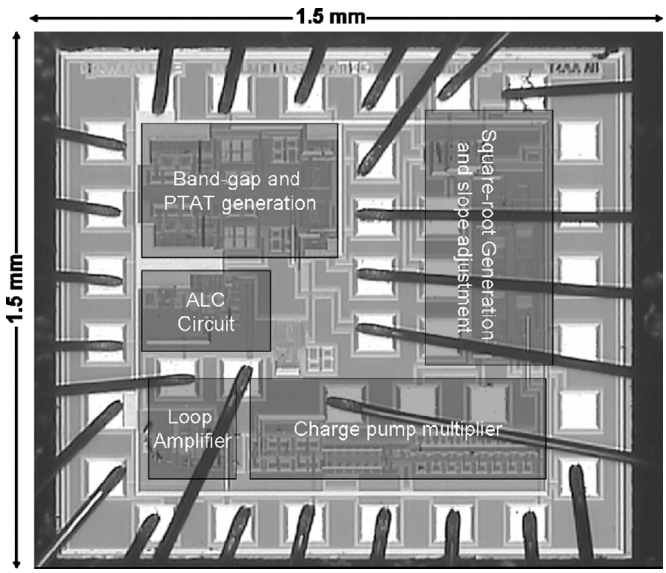

Fig. 19. Die picture of the interface IC.

VI. ERROR SOURCES IN THE COMPENSATION SCHEME

According to (2), any error in generating the bias voltage is translated to a frequency error. The accuracy of the parabolic TC scheme is limited by the inaccuracy of the bandgap reference and the PTAT generator, mismatches in the scaling amplifiers (including feedback resistors), and the inaccuracy of the square-root generator. Simulation predicted an overall variation of about 18 ppm over the temperature range of 25 °C to 125 °C with the parabolic compensation circuit. The measured variation was about 2 times larger. This is most likely because the effect of the opamp mismatch and resistor mismatch was

unaccounted in the simulation. By introducing a mismatch in the opamps, the overall simulated variation was increased to $\sim$25 ppm, a number that is closer to the measured variation. To estimate the worst-case error analytically, one should account for each of the error sources.

An analysis of the different error sources reveals that the opamp offset and the bandgap V_{BE} curvature contribute most to the total error. Hence, in order to achieve further performance gains, the accuracy of the bandgap and the PTAT circuits should be improved by the use of curvature compensation techniques [16] and the offset in the amplifiers should be minimized using standard offset cancellation techniques [17]. Using these techniques, the temperature stability can potentially be improved to sub-10 ppm, albeit at the cost of increased power consumption.

VII. Conclusion

In this paper, we have demonstrated the feasibility of electronically temperature compensated reference oscillators based on capacitive micromechanical resonators. Temperature compensation schemes that exploit the electrostatic frequency tuning characteristic of capacitive MEMS resonators have been developed in a standard 2P3M CMOS process. A temperature drift of 39 ppm was measured over 100 °C for the best compensation scheme, which represents a performance gain of over 70X over an uncompensated oscillator. The accuracy limit of the compensation technique has been analyzed and techniques for performance gains suggested.

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